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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,170	09/08/2003	Yoshiharu Hirakata	07977-241003	9943

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EXAMINER	
NHU, DAVID	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 01/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,170	HIRAKATA ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) *1-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *56-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/730,417; 09/046,198.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0104*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAIL ACTIONS

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 56-99 are rejected under U.S.C 103(a) as being unpatentable Background of Invention (BOI) in view of Majima et al (5,592,318).

Regarding claims 56, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: planaring an insulating film formed over a substrate 205 having an isulating surface; forming electrodes 206 on the insulating film; forming an insulating layer so as to cover the electrodes.

BOI fails to teach planarizing surfaces of the electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other, thereby filling boundary portions between the electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 57-59, see BOI, page 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Regarding claim 60, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: planaring an insulating film formed over a first substrate 205 having an isulating surface; forming stripped electrodes 206 on the insulating film; forming an insulating layer so as to cover the electrodes.

BOI fails to teach planarizing surfaces of the stripped electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the stripped electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the stripped electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other, thereby filling boundary portions between the stripped electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 61-63, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the

same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Regarding claims 64, 69, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: forming semiconductor elements 206, 207 over a substrate 205 having an insulating surface; forming an interlayer insulating film over the semiconductor elements; planaring the interlayer insulating film; forming pixel electrodes 208, 209 that arte electrically connected to the respective semiconductor elements on the interlayer insulating film; forming an insulating layer so as to cover the pixel electrodes.

BOI fails to teach planarizing surfaces of the pixel electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the pixel electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the pixel electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other, thereby filling boundary portions between the pixel electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 65-68, 70-73, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the

same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Regarding claims 74, 80, 86, 93, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: forming electrodes 208, 209 over a substrate 205 having an insulating surface; forming stripped electrodes 208, 209 over a substrate 205; forming semiconductor elements 206, 207 over a substrate 205 having an insulating surface; forming pixel electrodes 208, 209 that arte electrically connected to the respective semiconductor elements; forming semiconductor elements arranged in matrix form over a substrate 205.

BOI fails to teach forming a DLC film to cover the pixel electrodes; forming an insulating layer on the DLC film; planarizing the insulating layer so that a surface of the DLC film and a surface of the insulating layer become flush with each other, thereby filling boundary portions between the stripped/pixel electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the steps of forming a DLC film to cover the pixel electrodes; forming an insulating layer on the DLC film; planarizing the insulating layer so that a surface of the DLC film and a surface of the insulating layer become flush with each other, thereby filling boundary portions between the stripped/pixel electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 75-79, 81-84, 87-92, 94-99, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Matsubara'081, Hirakata'055, Hirakata'645 are cited as of interest.

4. A shortened statutory period for response to this action is set to expired 3 (three) months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).

5. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (703) 306- 5796. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu

January 5, 2004